Day 1 - Western Gateway Building - UCC				
Registration: 8:30 - 9:00 a.m. in the Atrium, Western Gateway Building, UCC				
Session	**Time**	**Presentation**	**Author**	**Affiliation**
Morning Session	**Co-chairs: Prof. Rao Tummala and Prof. Cian Ó Mathúna**			
Session 1	**Theme: Advanced packaging session 1**			
Plenary talk	**9:00 - 10:00 a.m.**	**Emergence of Glass Panel Packaging and 3D Glass Panel Embedded Package For Superior Bandwidth**	**Prof. Rao Tummala**	**IBM, Georgia Tech, Retd**
Paper	10:00 - 10:25 a.m.	Physical design enablement of 3 dies stacked 3D-Ics	Mohamed Naeim	IMEC
Paper	10:25 - 10:50 a.m.	Impact of Super-long-throw PVD on TSV Metallization and Die-to-Wafer 3D Integration Based on Via-last	Jiayi Shen	Tohoku University
Invited talk	**10:50 - 11:20 a.m.**	**Micro Transfer Printing**	**Alin Fecioru**	**Xceleprint**
Invited talk	**11:20 - 11:50 a.m.**	**Power Electronics Packaging**	**Dr. Jayakrishnan Chandrappan**	**CSA Catapult, UK**
Paper	11:50 - 12:15 p.m.	Parallelized Serial Daisy Chain Structure for Continuous In Situ Monitoring of Defect Formation	Andrew Ferris	Sandia Labs
Lunch	*12:15 - 2:00 p.m.*	***Lunch***		

Afternoon Session	**Co chairs: Prof. Rao Tummala and Prof. Cian Ó Mathúna**			
Session 2	**Theme: Advanced packaging session 2**			
Paper	2:00 - 2:25 p.m.	Chiplet Set For Artificial Intelligence	Joshua Stevens	NCSU
Paper	2:25 - 2:50 p.m.	Patterned InterVia for Heterogeneous Integration of III-V devices onto silicon photonics using micro-Transfer Printing	Ali Uzun	Tyndall
Paper	2:50 - 3:15 p.m.	3DIC integration with D2D bump-less Cu bonding	Ali Roshanghias	Silicon Austria Labs
Paper	3:15 - 3:40 p.m.	Fast, accurate assembly-level physical verification of 3DIC packages	Nermeen Hossam	Siemens
Break	*3:40 - 4:00 p.m.*	***Tea break***		
Invited talk	**4:00 - 4:30 p.m.**	**IC and photonic device fabrication and packaging services**	**Dr. Romano Hoofman**	**IMEC**
Invited talk	**4:30 - 5:00 p.m.**	**Electrical Interposers for 2.5D and 3D Integration**	**Dr. Gunnar Böttger**	**Fraunhofer IZM**
Paper	5:00 - 5:25 p.m.	A study on a tether-less approach towards Micro-Transfer-Printing of large-footprint power micro-inductor chiplets	Somnath Pal	Tyndall
Paper	5:25 - 5:50 p.m.	High performance, multi-layered, 2.5D interposer for RF Applications	Matthew Jordan	Sandia Labs

Day 2 - Western Gateway Building - UCC				
Registration: 8:30 - 9:00 a.m. in the Atrium, Western Gateway Building, UCC				
Morning session	**Co chairs: Colette Maloney and Prof. Peter O'Brien**			
Session 3	**Theme: European Chips Act and pilot lines**			
Plenary talk	**9:00 - 9:30 a.m**	**EU Chip act**	**Colette Maloney**	**European Commission**
Invited talks	**9:30 - 10:00 a.m.**	**European Packaging Pilot Line**	**Peter O'Brien**	**Tyndall**
Session 4	**Theme: Hybrid Bonding, test metrology and Thermal Management**			
Invited talk	10:00 - 10:30 a.m.	**Product Manager for Hybrid Bonding**	Jonathan Abdilla	Besi
Paper	10:30 - 10:55 a.m.	Cu Electrode Surface Features and Cu-SiO2 Hybrid Bonding	Murugesan Mariappan	Tohuku University
Paper	10:55 - 11:20 a.m.	Efficient Test Pattern Generation for Large Numbers of Inter-Die Interconnects in Chiplet-Based Packages	Slimane Boutobza	Cadence
Paper	11:20 - 11: 45 a.m.	Review of Hybrid Integration Techniques for integrating III-V onto Silicon	Erik Masselink	Gatech
Paper	11:45 - 12: 10 p.m.	Thermal cycling and fatigue life analysis of a GaN wide-bandgap laterally conducting power packaging	Pouria Zaghari	NCSU
Paper	12:10 - 12:35 p.m.	SiGe BiCMOS Technology with Embedded Microchannels based on Cu Pillar PCB Integration Enabling sub-THz Microfluidic Sensor Applications	Emre Can Durmaz	Leibniz Institute for High Performance Microelectronics, IHP
Lunch	***12:35 - 2:00 p.m.***	***Lunch***		

Afternoon Session	**Co chairs: Colette Maloney and Prof. Peter O'Brien**			
Plenary talk	**2:00 - 3:00 p.m.**	**Recent Advances in 3D Heterogeneous Integration Capabilities and Future Possibilities**	**Dr. Paul Fischer**	**Intel**
Session 5	**Theme: Emerging Technologies**			
Paper	3:00 - 3:25 p.m.	Thermal Management Strategies for Co-packaged Optics on Glass Interposers in Next-Generation Photonic Packaging	Parnika Gupta	Tyndall
Paper	3:25 - 3:50 p.m.	Effective release and transfer print of telecom wavelength devices	Hemalatha Muthuganesan	Tyndall
Paper	3:50 - 4:15 p.m.	Single-Mode Expanded-Beam Pluggable Module for Photonic Integrated Circuits	Kamil Gradkowski	Tyndall
Paper	4:15 - 4:40 p.m.	Development of an Ultra High Density Electrical Interposer for 2.5D Co-Packaging of a Silicon Photonic MEMs Chip	Arun Kumar Mallik	Tyndall
Social event / Gala dinner	***6:00 - 10:00 p.m.***	***Gala Dinner at the River Lee Hotel***		
Day 3 - Tyndall National Institute				

Morning Session	**Session Co-chairs: Prof. Peter Ramm and Dr. Kafil Razeeb**			
Session 6	**Theme: System integration and thermal management**			
Tour	9:00 - 10:00 a.m.	**Tyndall Tour**		
Plenary talk	**10:00 - 10:45 a.m**	**TBC**	**Mark Gerber**	**ASE Global group**
Break	***10:45 - 11:00 a.m.***	***Tea***		
Invited talk	**11:00 - 11:30 a.m.**	**Integrated biomedical systems**	**Stefan Andersson-Engels**	**Tyndall**
Invited talk	**11:30 - 12:00 p.m.**	**3D integration for Quantum Computing**	**Prof. Ryoichi Ishihara**	**TU Delft**
Paper	12:00 - 12:25 p.m.	Thermal insulation in superconducting flip-chip assemblies	Joel Hätinen	VTT
Paper	12:25 - 12:50 p.m.	Measurement Point Selection Algorithms for Testing Power TSVs	Koutaro Hachiya	Teikyo Heisei University, Japan
Lunch	**12:50 - 2:00 p.m.**	***Lunch***		